PROPOSAL TO SETUP INTEL UNNATI MULTI-DISCIPLINARY LABS

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Contents

Executive Summary

India aims to become a $1 trillion digital economy by 2025, and this requires significant investment in 21st century infrastructure and software capabilities.

The value pool is fundamentally shifting away from legacy technologies and towards digital—automation, cloud, cybersecurity, mobile, artificial intelligence (AI), 3-D printing, internet of things (IoT), big data analytics, and social media—at a pace even faster than anticipated just a few years ago. To emerge asan Information Technology and Business-Process Management (IT-BPM) leader, India needs to preparepeople to develop advanced capabilities in these technologies.

Enhancing the curriculum in higher education so that students and faculty are equipped with these data-centric skills is an important foundational element to make progress on this digital transformation journey.

To propel India's digital economy transformation, it is imperative that the higher education system in the country bridges this gap by developing new curricula and offering courses in emerging technologies. The National Education Policy 20201 recognises this and stresses the need for greater industry-academic linkages, and for higher education institutions to focus on research and innovation.

This proposal dwells in depth on how **Intel® Unnati Program** can keep pace with fast changing industry needs andexpectations and provide the academic institutions capability in the futuristic technology at an affordable investment and in a definitive time. The **Intel® Unnati Program** spurs the intelligent and exploratory mind of the academician and provides a canvas for the searching mind to create innovative assets.

Introduction

Artificial Intelligence has unleashed a new era of creativity and ingenuity. Today,Intel® technologies power some of the most promising AI use cases in business,society, and research. From massive cloud to tiny device, Intel turns the promise ofa transformative AI model into a global-scale reality.

Intel's portfolio of Xeon® scalable processors, combined with AI-optimised FPGAs, VPUs, memory and storage technologies, and software solutions ease the processfor deploying AI and data analytics in real-world applications.

Intel is committed to unlocking the promise of AI. To drive AI innovation, Intel ismaking strategic investments spanning R&D, technology, and partnerships with business, government, academia and community groups.

Identified Need

Industry and Education providers must collaborate to offer a significant curriculum, right training of skills,

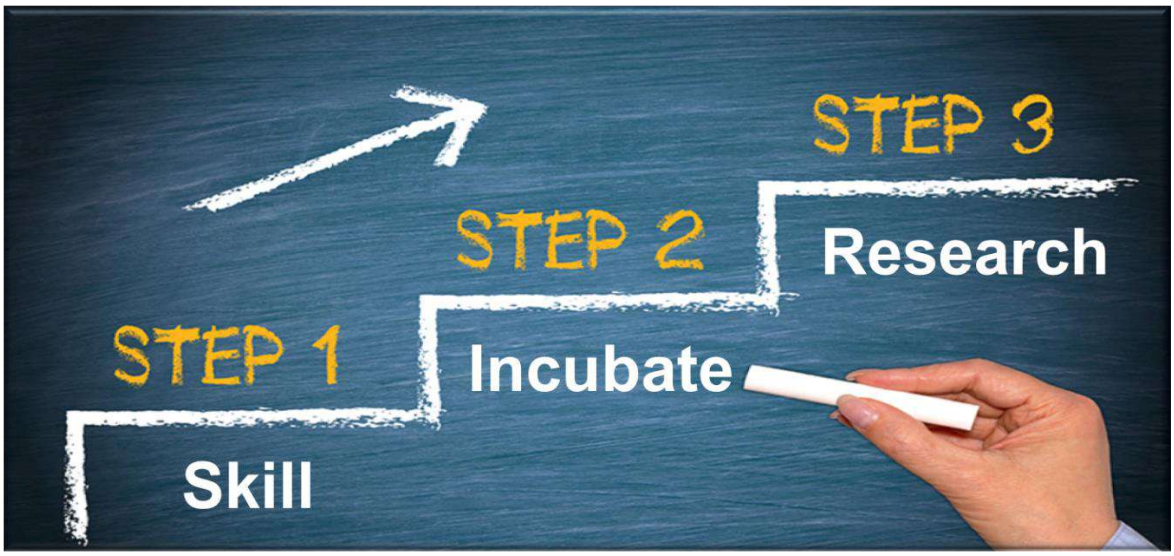
enhance the job opportunities and gain the hands-on experiential learning quotient in education. By gaining

information on the job roles, job needs, matching of skills imparted to job functions increases the transparency.

The objectivity in performance measurement must be created.

The integrated management of education for the employment activities of various stakeholders involves youth in aligning the choices with employment opportunities, create trust between the employer, educator, and youth.

Hence, the need of the hour is to ensure that there is continuous interaction and integration of efforts between the industry and academic institutions. The steps for growth of the integrated model of skill education is depicted here under:



Hence, it is imperative that the academic institutions in addition to the current curricula that they are providing in their traditional approach, needs to adopt additional skill development capabilities which takes all the students and the faculty together across these three steps of future readiness.

To support and extend the solution, **Intel Unnati Program** is the need of the hour for various skill development programs. The primary aim of any premier education institution is to create capability amongst students to become successful by adopting latest technologies and acquires skills that enable them to help the enterprises reach goals efficiently. However, striving for this type of excellence is often easier said than done. **Intel Unnati Program** is a key component of success in this direction.

What is INTEL Unnati Program

With the Intel® Unnati Program, you can keep pace with fast changing industry needs and expectations.

It will help Institutes

- **Equip your students with industry relevant data centric skills**
  In this age of data explosion, there is immense opportunity. Give your students the edge by equipping them with data-centric skills that will help them glean better insights and develop high-value solutions.

- **Unleash your students' creative potential**
  We, in India, have an incredible opportunity to unleash the creative potential of the largest student population in the world by training them in the right skills to drive India's digital transformation.

- **Build a strong reputation**
  With an Intel co-branded lab, you can be recognized as an institute that is committed to train your students in the latest technology to prepare them for industry and focus on faculty development.

- **Build capability for the long term**
  Establish your leadership and maintain it with the help of our System Integrator associates, who will get you Intel's recommendations for end-to-end Technology Labs set up, course content, and the training to go with it.

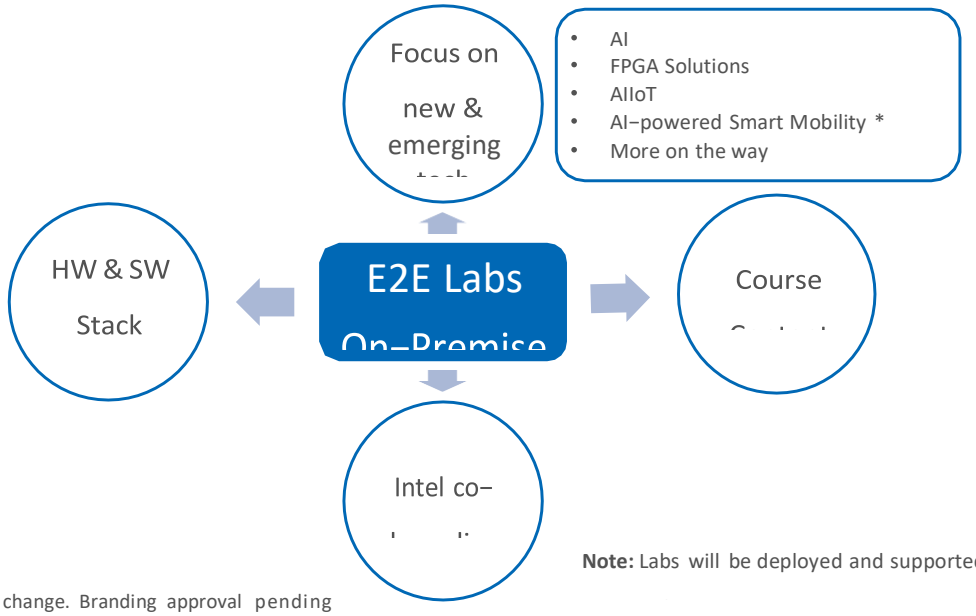
- **Leverage our System Integrator Associate Network**
  Be it training, customizations of your labset up, or your maintenance and support requests, you can rely on our strong System Integrator Associate Network for all your needs

- **Showcase New Skills**
  Students are awarded an Intel co-branded certificate at the completion of their course.

- **Coursework that Enables Learning by Doing**
  With an emphasis on hands-on exercises, the course covers Machine Learning, Deep Learning, and deploying Models using Intel Distribution of OpenVino™ toolkit on modern Intel® architecture.

- **Custom Lab Deployments**
  Our System Integrator associates will assist you for customizations to your lab setup and training content to suit your needs.

Intel® Unnati - Data-Centric Labs in Emerging Technologies



Note: Labs will be deployed and supported by Intel–

* Name subject to change. Branding approval pending

HIGH LEVEL LAB DESIGN

On-Premise

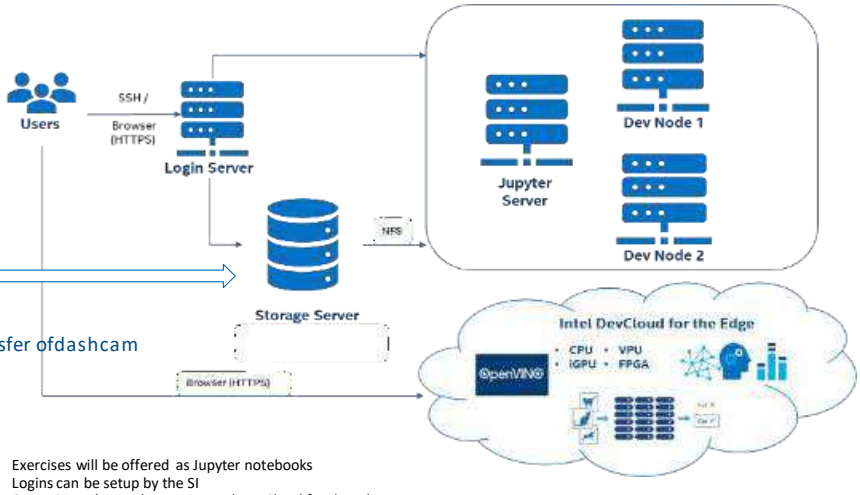
In-Vehicle

ADAS Collision Avoidance System (CAS)

Dashcam with local storage

Cloud-based subscription

Periodic transfer of dashcam data to



- Exercises will be offered as Jupyter notebooks
- Logins can be setup by the SI
- OpenVino Labs can be run on Intel DevCloud for the Edge
- Job scheduling, if needed, will be setup by the SI during deployment using PBS / Slurm /Kubernetes

Course Details

AI/ML/ADAS:

Machine Learning on Modern Intel Arch (Duration: Approx15hrs)		
Prerequisites: • Python programming • Calculus • Linear algebra • Statistics	**Learning Outcomes:** • Supervised learning algorithms • Key concepts like under – and over–fitting, regularization, and cross – validation • How to identify the type of problem to be solved, choose the right algorithm, tune parameters, and validate a model • Unsupervised learning	**Lab Exercises:** • Supervised Learning and K Nearest Neighbors • Train Test Splits, Cross Validation, and Linear Regression • Regularization and Gradient Descent • Logistic Regression and Classification Error Metrics • Clustering Methods
Deep Learning on Modern Intel Architecture (Duration: Approx18 hrs)		
Prerequisites: • Python programming • Calculus • Linear algebra • Statistics • Machine Learning Course	**Learning Outcomes:** • Techniques, terminology, and mathematics of DL • Fundamental neural network architectures, feedforward networks, convolutional networks, and recurrent networks • How to appropriately build and train models • Various deep learning applications • How to use pre –trained models for best results	**Lab Exercises:** • Handwritten Image Detection with Keras using MNIST data • Building a CNN to classify images in the CIFAR – 10 Dataset • Transfer Learning using MNIST data • Using Pre –Trained Models • Classifying CIFAR–10 with Data Augmentation • Hands on E2E workflow using an image classification problem.
ADAS Alert Analysis using Intel Distribution of OpenVino Toolkit (Duration: Approx10 hrs)		
Prerequisites: • Python programming • Calculus • Linear algebra • Statistics • Machine Learning Course • Deep Learning Course	**Learning Outcomes:** • Learn about Intel® Distribution of OpenVino toolkit for DL inference • Real–time data analysis	– Collect real –time data from N vehicles over a period of 30 days, with ADAS sensors (Dashcams optional) **Lab Exercises:** • Normalization of real –world data from sensors on t across time • User–specific data analysis (alert types, behaviour categorization) • Population rank based on metrics • **Identification of hotspots on road network, ahead of possible accidents (project)** • **Use AI/ML to identify near- accident events from large video footage (project - optional with Dashcam)**

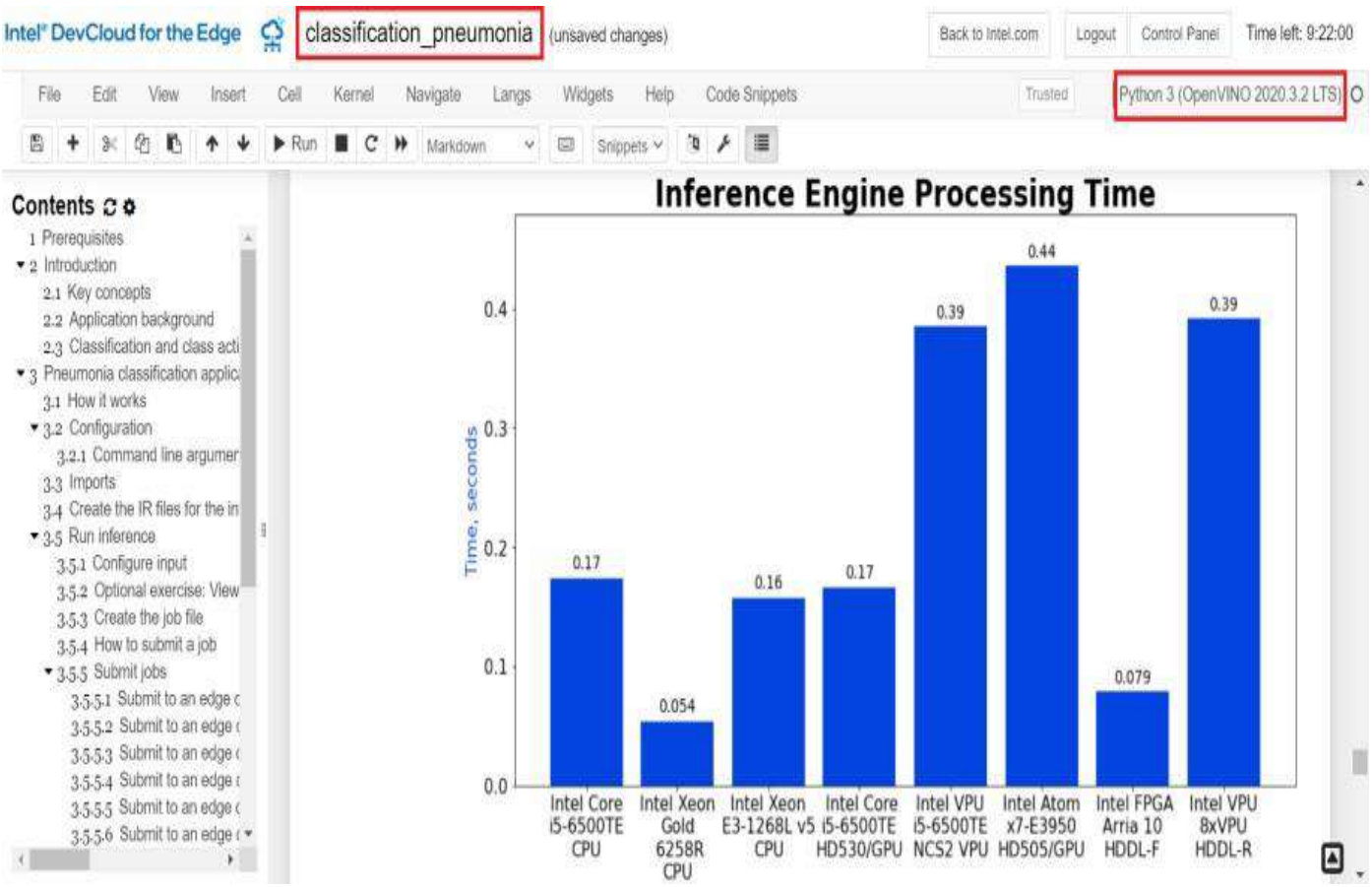
Digital Logic and Embedded Systems:

Minimum Suggested Specifications for 30 Users		
Server/Workstations 15 (minimum 10) x Intel® Core™ i3 processor based PCs with at least 4 GB RAM	**Boards** 10 x DE10-Lite* 2 x DE10-Nano* 2 x DE1-SoC* 1 x DE10-Standard*	**Software** Intel® Quartus® Lite with FPGA libraries supported along with ModelSim* FPGA Starter editionand Intel® SoC Embedded Development Suite (SoC EDS) standard edition and Intel® HLS Compiler
Project Development Kits *for semester long capstones and senior designs* Self Balancing Robot: *https://www.terasic.com.tw/cgi-bin/page/archive.pl?Language=English&CategoryNo=238&No=1096* Servo Motor Kit: *https://www.terasic.com.tw/cgi-bin/page/archive.pl?Language=English&CategoryNo=238&No=1028* A-Cute Car Robotic Kit: *https://www.terasic.com.tw/cgibin/page/archive.pl?Language=English&CategoryNo=238&No=1018&PartNo=1* Terasic Spider: *https://www.terasic.com.tw/cgi-bin/page/archive.pl?Language=English&CategoryNo=238&No=994&PartNo=6* Multi Touch LCD Module: *https://www.terasic.com.tw/cgi-bin/page/archive.pl?Language=English&No=653*		

Digital Logic		
Prerequisites: • Fundamentals of Electronics • Boolean Logic • Any Programming Language	**Learning Outcomes:** • Combinational and Sequential logic • Key logic elements - storage clocks and memory • How to implement finite state machines in circuitry • How to write, compile, synthesize and download hardware designs for FPGAs	**Lab Exercises:** • Switches, Lights and Multiplexers, Numbers and displays • Latches, FFs & Registers, Counters, Timers and Real-time clocks • Adders, Subtractors and Multipliers, Finite State Machines • Memory blocks, A Simple Processor, An Enhanced Processor • Implementing Algorithms in hardware and Basic DSP
Embedded Systems		
Prerequisites: • Familiarity with the Bresenham line-drawing algorithm • Linux Kernel modules	**Learning Outcomes:** • Writing Linux Kernel modules that use device drivers • Designing user level programs that use available hardware resources • Graphics and animation on a VGA display • Use the ADXL345 accelerometer	**Lab Exercises:** • Get started with Linux • Develop Linux Programs that communicate with FPGAs • Character device drivers and Using Character device drivers • Use ASCII graphics for animation & Intro to graphics & animation • Use the ADXL 345 accelerometer • Introduction to audio and multithreaded applications
Artificial Intelligence		
Prerequisites: • Digital Logic course • Embedded Systems course	**Learning Outcomes:** • Using the Intel SDK for OpenCL applications • Improvements OpenCL kernels can offer in various situations • How FPGAs can be used to accelerate AI inference	**Lab Exercises:** • Get started with the Intel SDK for OpenCL applications • Accelerating Computer Vision Techniques • Lane detection for Autonomous driving • Classification of Handwritten digits – Linear Classifier • Classification of Handwritten digits – CNN Classifier
Acceleration Stack for Xeon CPU with FPGAs		
Prerequisites: • Basic Understanding of FPGAs	**Learning Outcomes:** • Know the basics of using RTL tools and methods to develop an accelerator function for the FPGA that interacts with the acceleration stack • How to develop an AFU for the FPGA • Understand the CCI-P that connects the accelerator function • Use the OPAE to interact with the accelerator function	**Lab Exercises:** • Creating a host application • Simulating with ASE • Add a scratch register to AFU and host application • Generate the AFU bitstream to configure the FPGA

Value Adds

Access to Intel DevCloud for the Edge



FPGA Project development Kits

(for semester long capstones and senior designs)

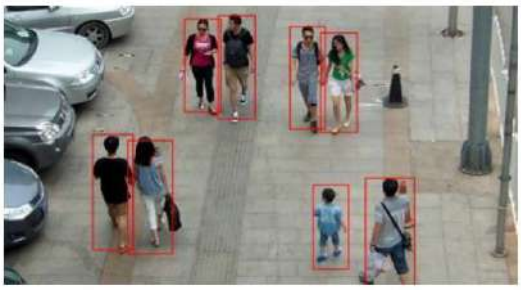
- Self- Balancing RobotServo Motor Kit
- A-Cute car robotic kitTerasic Spider
- Multi Touch LCD Module

IoT Reference Implementations

https://software.intel.com/content/www/us/en/develop/topics/iot/reference-mplementations.html

Social Distance Detection:

Human & Vehicle Detection:



Conclusion

Intel Unnati Program for Futuristic Technologies ensures that the academic institutions equip themselves with the ever-changing technology tools and capabilities on one hand and skill the students with such futuristic technologies. The program creates capability within the academic institution to address the dual requirement of being a part of innovative growth and the skilling of students calls for a setting up of Center of Excellence by providing the platform for doing both.

This proposal details how **Intel Unnati Program** provide the academic institutions capability in the futuristic technology at an affordable investment and in a definitive duration. By engaging in the program the academic institutions, their faculty, research scholars, and the students stand to gain by way of increased traction from the industry for research, opportunity for the faculty and research scholars to present papers and create innovative re-usable solutions, and students to increase their employability by acquiring globally recognized skills.

We look forward to being partner in your esteemed institution's journey in achieving academic excellence and create a platform for regular industry academician interaction.

We are authorized to present this proposal to you as Intel authorized partner and accordingly submit this proposal for your kind consideration and approval.

Signature of Authorized Signatory:

Name:

Designation:
Company Name and Seal: Date:

Bill of Materials for AI Starter Labs

1 x Node (Minimum 1 PhysicalCore and 8GB RAM per user)	• Dual Intel® Xeon® Gold 5318Y, 24 cores, 2.1 GHz base frequency, 36 MB cache • 256 GB Memory: 16 x 16 GB of 2993 MHzDDR4 ECC Registered Memory • 1 TB SSD	• Ubuntu* 18.04 • Intel® oneAPI Base Toolkit • Intel® AI Analytics Toolkit • Horovod* + Intel® MPI (optional, for distributed DL training with TensorFlow*) • JupyterHub* and JupyterLab* • Keras*, ipykernel*, Seaborn* + other packages as required by exercises Note: Check *https://software.intel.com/ containers* For available AI containers
1 x Login + StorageServer	• Intel® Xeon® Silver 4310, 12 cores, 2.1 GHz base frequency, 18 MB cache, 128 GB RAM • At least 10 GB disk space per user (Capacity should based on estimate of total users who would utilise this lab)	• Ubuntu* 18.04
+ Network Router with 4 RJ45 1Gbps Port, Power Delivery Unit (PDU), Patch Cables and Power Cable		
OpenVino™ labs will be run on Intel® DevCloud for the Edge		

Bill of Materials for AI Builder Lab

AI Builder Lab Infrastructure	Minimum Suggested Specifications for 30 Users		
For institutions that are seeking to go beyond lab exercisesand investing in the next generation of AI Builders	3 x Nodes (Minimum 2 PhysicalCores and 8GB RAMper user) Note: You could use 1 node as the Jupyter* server	• Dual Intel® Xeon® Gold 5318Y, 24 cores, 2.1 GHz base frequency, 36 MB cache • 256 GB Memory: 16 x 16 GB of 2993 MHzDDR4 ECC Registered Memory • 1 TB SSD	• Ubuntu* 18.04 • Intel® oneAPI Base Toolkit • Intel® AI Analytics Toolkit • Horovod* + Intel® MPI (for distributed DLtraining with TensorFlow*) • Intel® Extension for PyTorch* (IPEX) • Intel® Distribution of OpenVINO™ Toolkit Note: Check https://software.intel.com/containers for available AI conta Jupyter* Server: • Ubuntu* 18.04 • JupyterHub* and JupyterLab* • Keras*, ipykernel*, Seaborn* + other libs as required by exercises
	1 x Storage Server	• Rackmount 4 - Bay Network* Attached St with at least 50GB disk space per user (Capacityshould be based on estimate of total users whowould utilise this lab)	
	1 x Login Server	• Intel® Xeon® Silver 4310, 12 cores, 2.1 GHz base frequency, 18 MB cache, 128 GB RAM, 5 SSD	• Ubuntu* 18.04
	+ Network Router with 1Gbps Ports, Network Switch, Rack Cabinet, Power Delivery Unit (PDU), Patch Cablesand Power Cable		
	+ Software for job scheduling and queueing		
	OpenVino™ labs will be run on Intel® DevCloud for the Edge		

4 - 8 x Nodes	Dual Intel® Xeon® Gold 6330, 28 cores, 2.0 base frequency, 42 MB cache • 256 GB Memory: 16 x 16 GB of 2933 MHz ECC Registered Memory • 1 TB SSD	• Ubuntu* 18.04 • Intel® oneAPI Base Toolkit • Intel® AI Analytics Toolkit • Horovod* + Intel® MPI (for distributed DLtraining with TensorFlow*) • Intel® Extension for PyTorch* (IPEX) • Intel® Distribution of OpenVINO™ Toolkit Note: Check *https://software.intel.com/ containers* for available AI containers
1 x FPGA InferenceNode (only Qualified† Servers)	• Intel® Xeon® Silver 4314, 16 cores, 2.4 GHz base frequency, 24 MB cache • 128 GB Memory: 8 x 16 GB of 2667 MHz DDR4ECC Registered Memory • 1 TB SSD • 1-2 Intel® Programmable Acceleration Cardwith Intel Arria® 10 GX FPGA†	• Ubuntu* 18.04 • Intel® oneAPI Base Toolkit • Intel® AI Analytics Toolkit • Intel® FPGA Add-On for oneAPI Base Toolkit • Intel® Distribution of OpenVINO™ Toolkit(LTS Release
1 x VPU InferenceNode	• Intel® Xeon® Silver 4314, 16 cores, 2.4 GHz base frequency, 24 MB cache • 128 GB Memory: 8 x 16 GB of 2667 MHz ECC Registered Memory • 1 TB SSD • 1-2 Intel® Vision Accelerator Design With Movidius™ Vision Processing Unit with supportfor up to 8 VPUs	• Ubuntu* 18.04 • Intel® oneAPI Base Toolkit • Intel® AI Analytics Toolkit • Intel® Distribution of OpenVINO™ Toolkit
1 x Login Server	• Intel® Xeon® Silver 4310, 12 cores, 2.1 GHz base frequency, 18 MB cache, 128 GB RAM, SSD	• Ubuntu* 18.04
1 x Storage Server	• TrueNAS* 1U 120 TB or equivalent	• TrueNAS* Open Storage OS
Ethernet Cards	• Intel® Ethernet 700 Series Network Adapters • *Upgrade to Intel® Ethernet 800 Series, which offers upto 100GbE, when available*	
+ Network Router with 25-100Gbps Ports, Power Delivery Unit (PDU), Patch Cables and Power Cable		
+ Software for job scheduling and queueing		

Important notes relating to all AI Lab Configurations

1. If Network File System (NFS) is installed, then all Intel software tools need to be installed only once through anyof the compute nodes on to a network location visible to all nodes. If you don't have NFS, then only the runtime components of Intel tools need to be installed on the hard drive of every node.
2. Initialise MPI environment first before installing Horovod*. (source setvars.sh)

Minimum Suggested Specifications for 30 Users		
Server/Workstations • 15 (minimum 10) x Intel® Core™ i3 processorbased with at least 4 GB RAM	**Boards** • 10 x DE10-Lite* • 2 x DE10-Nano* • 2 x DE1-SoC* • 1 x DE10-Standard*	**Software** • Intel® Quartus® Lite with FPGA libraries supported a with ModelSim* FPGA Starter editionand Intel® S Embedded Development Suite (SoC EDS) standard edition and Intel® HLS Compiler
Project Development Kits *for semester long capstones and senior designs* • Self Balancing Robot: *https://www.terasic.com.tw/cgi-bin/page/archive.pl?Language=English&CategoryNo=238&No=1096* • Servo Motor Kit: *https://www.terasic.com.tw/cgi-bin/page/archive.pl?Language=English&CategoryNo=238&No=1028* • A-Cute Car Robotic Kit: *https://www.terasic.com.tw/cgibin/page/archive.pl?Language=English&CategoryNo=238&No=1018&PartNo=1* • Terasic Spider: *https://www.terasic.com.tw/cgi-bin/page/archive.pl?Language=English&CategoryNo=238&No=994&PartNo=6* • Multi Touch LCD Module: *https://www.terasic.com.tw/cgi-bin/page/archive.pl?Language=English&No=653*		

FPGA Courses

1) Digital Logic
2) Computer Organisation
3) Embedded Systems

Bill of Materials for FPGA and Artificial Intelligence Lab

Minimum Suggested Specifications for 30 Users		
Server/Workstations • Tools/License Server: Intel® Core™ i7/i9 orIntel® Xeon processor, 64 GB RAM, 500 GBSATA HDD running Linux OS, 24" Monitor, Keyboard and Mouse *Optional:* Graphics Card • 1 x Qualified Server for housing the Intel® Programmable Acceleration Card (PAC): Refer to *Qualified Servers* list below • 15 (minimum 10) x Intel® Core™ i3 processor based PCs with at least 4 GB RAM for server-based license access	**Acceleration Cards** • 2 x Intel® Arria® 10 FPGAPAC *or* • 1 x Intel® Arria® 10 FPGA PAC and 1 x Intel® Stratix® 10 FPGA PAC (D5005)	**Software** • Intel® Quartus® Standard DesignSoftware and Intel® for OpenCL™ is included • Intel® Distribution of OpenVINO™Toolkit • Intel® oneAPI Base Toolkit • Intel® FPGA Add-on for oneAPIBase Toolkit • Intel® Acceleration Stack (supports OpenCL™, DPC++, RTL based descriptions)
Project Development Kits *for semester long capstones and senior designs* • Intel® Arria® HAN Pilot: *https://www.terasic.com.tw/cgi-bin/page/archive.pl?Language=English&CategoryNo=228&No=1133* • Intel® Arria® Flik: *https://www.terasic.com.tw/cgi-bin/page/archive.pl?Language=English&CategoryNo=228&No=1237* Users can also try out the oneAPI or FPGA DevCloud for a limited period of time: • Intel® DevCloud for the Edge: *https://devcloud.intel.com/edge/home* • Intel® DevCloud for oneAPI: *https://devcloud.intel.com/oneapi* • FPGA DevCloud: *https://software.intel.com/content/www/us/en/develop/tools/devcloud/fpga.html* Qualified Servers for Intel® FPGA PAC: • With Intel® Arria® 10 GX: *https://www.intel.com/content/www/us/en/programmable/products/boards_and_kits/dev-kits/altera/acceleration-car arria-10-gx/buy.html* • D5005: *https://www.intel.com/content/www/us/en/programmable/products/boards_and_kits/dev-kits/altera/intel- fpga-pac-d5005/buy.html*		

Minimum Suggested Specifications for 30 Users		
Server/Workstations • Tools/License Server: Intel® Core™ i7/i9 orIntel® Xeon processor, 64 GB RAM, 500 GBSATA HDD runn Linux OS, 24" Monitor, Keyboard and Mouse *Optional:* Graphics Card	**Boards and Cards** • 1 x Intel® Arria® 10 GX withADI* AD9371* • 1 x Intel® Stratix® 10 GX with ADI* AD9174* Select board based on required peripherals and connectors.	**Software** • Intel® Quartus® Standard DesignSoftware is included along with the development board
Project Development Kits *for semester long capstones and senior designs* • RFS: *https://www.terasic.com.tw/cgi-bin/page/archive.pl?Language=English&CategoryNo=225&No=1025* • ADC-FMC: *https://www.terasic.com.tw/cgi-bin/page/archive.pl?Language=English&CategoryNo=73&No=1193& PartNo=2#section* **Design Examples** • JESD204B Intel® Arria® 10 FPGA IP Design • JESD204B Intel® Stratix® 10 FPGA IP Design		